IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 09/976,708 §	Examiner: Trimmings, J.
Filed: October 12, 2001 §	Group/Art Unit: 2133
Inventor(s): §	Atty. Dkt. No: 5681-55500
Michael C. Dorsey §	

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Title: ASIC LOGIC BIST §
EMPLOYING REGISTERS §
SEEDED WITH §
DIFFERING PRIMITIVE §
POLYNOMIALS §
§
§

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal of February 28, 2005, Appellants present this Appeal Brief. Appellants respectfully request that this appeal be considered by the Board of Patent Appeals and Interferences.

I.   REAL PARTY IN INTEREST

The subject application is owned by Sun Microsystems, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at 901 San Antonio Road, Palo Alto, California 94303, as evidenced by the assignment recorded at Reel 012257, Frame 0867.

II.   RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III.   STATUS OF CLAIMS

Claims 1-33 are pending in the present application. Claims 1-33 stand finally rejected and are the subject of this appeal. A clean copy of claims 1-33, as on appeal (incorporating all amendments), is included in the Appendix hereto.

IV.   STATUS OF AMENDMEMNTS

An amendment to the claims has been filed subsequent to the final rejection. The Appendix hereto reflects the current state of the rejected claims.

V.   SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a built-in self-test controller. The built-in self-test controller (e.g., item 100, Fig. 1, page 5, line 11 to page 6, line 33) includes a logic built-in self-test engine (e.g., item 160, Fig.1 and Fig. 2, Page 7, lines 1-20) having a logic built-in self-test state machine (e.g., item 210, Fig. 2; page 7, lines 1-13), a pattern generator (e.g., item 230, Fig. 2, page 7, lines 1-13) that is seeded with a first primitive polynomial, and a multiple input signature register (e.g., item 220, Fig. 2, page 7, lines 1-13) that is seeded with a second primitive polynomial. The first primitive polynomial has

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a first number of bits while the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

Independent claim 8 is directed to a built in self-test controller. The built-in self-test controller (e.g., item 100, Fig. 1, page 5, line 11 to page 6, line 33) includes a means for executing a logic built-in self-test (e.g., item 160, Fig.1 and Fig. 2, Page 7, lines 1-20) having a pattern generator (e.g., item 230, Fig. 2, page 7, lines 1-13) that is seeded with a first primitive polynomial. The built-in self-test controller further includes a means for storing resulted of an executed logic built-in self-test ((e.g., item 220, Fig. 2, page 7, lines 1-13), the contents thereof being stored per a second primitive polynomial. The first polynomial has a first number of bits while the second polynomial has a second number of bits, wherein the second number is different from the first number.

Independent claim 12 is directed to an integrated circuit device. The integrated circuit device includes a plurality of memory components (e.g., items 190, Fig. 1, Page 5, lines 24-27), a testing interface (e.g., item 180, Fig. 1, page 5, line 29-31), and a logic built-in self-test controller (e.g., item 160, Fig.1 and Fig. 2, Page 7, lines 1-20). The logic built-in self-test controller includes a logic built-in self-test engine (e.g., item 110, Fig. 1 and Fig. 2, page 7, lines 1-20) including a logic built-in self-test state machine (e.g., item 210, Fig. 2; page 7, lines 1-13), and a pattern generator (e.g., item 230, Fig. 2, page 7, lines 1-13) seeded with a first primitive polynomial, and a multiple input signature register (e.g., item 220, Fig. 2, page 7, lines 1-13) that is seeded with a second primitive polynomial. The first primitive polynomial has a first number of bits while the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

Independent claim 22 is directed to a method for performing a logic built-in self-test. The method includes seeding a pattern generator (e.g., item 230, Fig. 2, page 7, lines 1-13) in a logic built-in self-test controller (e.g., item 160, Fig.1 and Fig. 2, Page 7, lines 1-20) with a first primitive polynomial, executing a logic built-in self-test using the

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contents of the pattern generator, and storing the results of an executed logic-built in self-test in a multiple-input signature register (e.g., item 220, Fig. 2, page 7, lines 1-13) utilizing a second primitive polynomial. The first primitive polynomial has a first number of bits while the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

Independent claim 29 is directed to a method for testing an integrated circuit device. The method includes interfacing the integrated circuit device (e.g., item 150, Fig 1, page 5, line 11 to page 6, line 33) with a tester and performing a logic built-in self-test. Performing the logic built-in self-test includes seeding a pattern generator (e.g., item 230, Fig. 2, page 7, lines 1-13) in a logic built-in self-test controller (e.g., item 160, Fig.1 and Fig. 2, Page 7, lines 1-20) with a first primitive polynomial, executing a logic built-in self-test using the contents of the pattern generator, and storing the results of an executed logic-built in self-test in a multiple-input signature register (e.g., item 220, Fig. 2, page 7, lines 1-13) utilizing a second primitive polynomial, and reading the stored results. The first primitive polynomial has a first number of bits while the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

VI.   GROUNDS OF REJECTION TO BE REVIEWED ON APEAL

1.   Claims 1, 3, 5, 8, 10, 22, 24 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara (U.S. Patent 6,629,281), in view of Kim (U.S. Patent 5,938,784), in view of Pouya, (U.S. Patent 6,701,476), and in further view of Udawatta (U.S. Patent 6,738,939).

2.   Claims 2, 9, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta and in further view of Bardell (U.S. Patent Number 4,959,832).

3.   Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Simpson (U.S. Patent 5,260,950), Wong (U.S. Patent 6,636,997), and Bogholtz (U.S. Patent 5,357,523).

4.   Claims 7, 11, and 28 are rejected under 35 U.S.C. § 103(a) as being patentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Rajski (U.S. Patent 5,991,909).

5.   Claims 6, 12, 14, 16, 17, 18, and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika (U.S. Patent 5,982,189).

6.   Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika and Bardell.

7.   Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika, Simpson, Wong, and Bogholtz.

8.   Claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika and Kim ('Kim 2') (U.S. Patent 6,148,426).

9.   Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of of Motika and Au (U.S. Patent 6,681,359).

10.   Claim 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika and

Rajski.

11.   Claim 26 is rejected under 35 U.S.C. § 103(a) as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Wong and Bogholtz.

12.   Claims 29, 31, 32, and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Rajski and in further view of Kim, Pouya, and Udawatta.

13.   Claim 30 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Rajski and in view of Kim.

VII.   ARGUMENT

A.   Claims 1, 3, and 5

The Examiner rejected claims 1, 3, and 5 as being unpatentable over McNamara in view of Kim, and Pouya, and in further view of Udawatta under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Independent claim 1 recites, in pertinent part:

"A built-in self-test controller, comprising … a pattern generator seeded with a first primitive polynomial; and a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial; wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number." (Emphasis added).

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In the Final Office Action, the Examiner admits that McNamara and Kim fail to teach the first and second polynomials being a certain number of bits, wherein the second polynomial has a number of bits different from the first. The Examiner also notes that Pouya suggests the polynomials be different polynomials, but does not specifically state they be different in the number of bits. However, the Examiner asserts that Pouya boasts of reduced test cost in column 1, lines 35-40, and further asserts that motivated as suggested, one with ordinary skill in the art would add the variable polynomial capabilities to the McNamara and Kim references in order to decrease test costs. Appellant submits that this suggestion by Pouya is not equivalent to a suggestion of first and second primitive polynomials having different numbers of bits, as recited in the independent claims.

The Examiner further states in the Final Office Action that Udawatta does teach the feature of a first primitive polynomial having a different number of bits than a second primitive polynomial, and cites Udawatta at column 2, lines 17-67 and column 3, lines 59-61. Column 3, lines 59-61 of Udawatta states:

"Also, the invention can support MISRs <u>with different polynomial sizes by the ability to add more logic and flip flops</u> to store larger polynomials." (Emphasis added).

While the above citation may teach MISRs that support different polynomial sizes, this citation is silent as to whether these different polynomial sizes are present in the same embodiment or in different embodiments. Appellant notes that the citation appears to suggest enlarging the MISRs by adding more logic and flip-flops for the purpose of storing larger polynomials, but submits that the citation does not suggest an embodiment having two or more MISRs of different sizes. Furthermore, Appellant notes that while the citation above states that MISRs can support different polynomial sizes (and thus may support variation in the size of a second primitive polynomial), Udawatta is silent about the size of the LFSR, any relation between the size of the LSFR and the plurality of

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MISRs, or the size of a first primitive polynomial stored within the LSFR. Accordingly, Appellant submits that Udawatta does not teach or suggest first and second primitive polynomials of different sizes as recited in the independent claims, and further submits that the cited references, taken singly or in combination do not teach or suggest all of the elements of the independent claims.

Appellant further notes that, in supporting the rejection, the Examiner cites column 3, lines 16-19 of Udawatta, which states:

"Also, one can address the issue of aliasing by increasing the length of the MISR, which has the effect of minimizing the aliasing effect." (Emphasis added).

However, column 1, line 65 to column 2, line 6 of Kim states:

"Since the number of flip-flops in the conventional BIST circuit, implemented using the LFSR and the MISR circuits of FIGS. 1 and 2, is dependant upon the number of inputs and outputs of the circuit to be tested, a circuit to be tested having a large number of inputs and outputs will require a corresponding large number of flip-flops on the LFSR and MISR test circuits. Consequently, the circuit real estate or overhead required for such a BIST circuit increases dramatically." (Emphasis added).

MPEP 2141.02 states that the prior art must be considered in its entirety, including disclosures that teach away from the claims. MPEP 2145 (X)(D)(2) states that references cannot be combined where the references teach away from their combination. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. In light of the above citations from Udawatta and Kim, as well as column 4, lines 32-37 of Kim, which states:

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"As described above, according to the present invention, the BIST circuit is implemented using the LFSR and the MISR which share a memory built in a circuit to be tested, and thus the area of the BIST circuit can be greatly reduced regardless of the number of inputs and outputs of the circuit to be tested." (Emphasis added),

Appellant submits that Udawatta and Kim teach away from their combination with each other and further submits that a combination of references including both Udawatta and Kim renders Kim unsatisfactory for its intended purpose (reducing the area required by the BIST circuit). Accordingly, Appellant submits that there is no suggestion or motivation to combine these references.

For at least these reasons, Appellant submits that the rejection of claim 1, as well as claims 3 and 5 (which depend from claim 1) is in error, and therefore respectfully requests reversal of the rejection.

B.   Claim 2

The Examiner rejected claim 2 as being unpatentable over McNamara in view of Pouya and Kim and in further view of Udawatta and Bardell under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 2 is dependent upon claim 1. For at least the reasons stated above in regard to claim 1, Appellant submits the rejection of claim 2 is in error and therefore respectfully requests reversal of the rejection.

C.   Claim 4

The Examiner rejected claim 4 as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Simpson, Wong, and Bogholtz under

35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant submits that the cited references, taken singly or in combination, do not teach or suggest all of the elements of claim 4, which in pertinent part recites:

"a step state entered into from the scan state and from <u>which the scan state is entered</u> <u>**unless**</u> the content of the pattern generator equals a predetermined <u>**vector**</u> <u>**count**</u>" (Emphasis added).

In the Final Office Action, the Examiner asserts that Wong teaches the states of scan, step, and complete in column 6, lines 26-50. Column 6, lines 26-50 of Wong states:

"Referring to FIG. 4, a flow diagram for a preferred process 400 of operating the system 100 in accordance with the present invention is shown. After the start 402 of the process 400, the scan path initializes 404 the state elements of the scan registers by flushing the scan path. During initialization, the state elements in the LRSCs 108.sub.1, 108.sub.2 and LNSCs 110.sub.1, 110.sub.2 are flushed to a zero state. This ensures that the last scan register 106.sub.6 in the functional path is in a 1-hot or 1-cold condition. Upon completion of initialization, the process 400 then disables update of all the LRSCs 406 by holding the clock enable off for state elements in the LRSCs 108.sub.1, 108.sub.2.

The process then performs 408 a certain number of system clocks to establish partially decoded values in the functional path based on an all zero encoded state. The PRPG 102 feeds 410 random data to the LRSCs 108.sub.1, 108.sub.2, but not to the LNSCs 110.sub.1, 110.sub.2. The process 400 then runs 412 the LBIST sequences until complete. The MISR 114 receives bit values which indicate test responses and produces 414 a unique signature. As shown in step 417, if the test is not completed, the process returns to step 410 to repeat the process until it is

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completed. The signature may be examined to determine the condition of the system 100, which ends 416 process 400."

The Examiner further states in the Final Office Action that Bogholtz teaches ending the BIST under the condition of comparing the pattern generator to a pre-set count, citing Fig. 10, 32, and column 8, lines 27-40. Column 8, lines 27-40 of Bogholtz states:

"Additionally, FIG. 10 illustrates circuitry that can be employed to allow for generation of the all zeros data pattern. A comparator 32 is implemented to receive and compare the outputs of the start register 18 and counter/LFSR 20. When the comparator 32 determines that the generated data pattern developed by the counter/LFSR 20 is the same as the seed data pattern, then zero output circuitry 34 forces the generated data pattern in the counter/LFSR 20 to all zeros. Further, when an all zeros data pattern is generated, the control circuitry can be programmed to send the next load control signal to the start register 18 one cycle later. Thus, the zero data pattern can be generated without skipping any data patterns in the predetermined sequence."

Appellant can find no teaching or suggestion of the step state as recited in claim 4 anywhere in Wong or Bogholtz, including in the above citations. In particular, Appellant can find no teaching or suggestion of a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count. Appellant further submits that none of the cited references, taken singly or in combination teach or suggest this limitation and that none of the cited references provides a teaching, suggestion, or motivation for adding this limitation and thus obtaining the combination of features recited in claim 4.

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In addition to the reasons above, Appellant notes that claim 4 depends from claim 1 and is thus also believed allowable for the reasons stated above in regard to claim 1.

For at least these reasons, Appellant submits that the rejection of claim 4 is in error, and respectfully requests reversal of the rejection.

D.   Claim 6

The Examiner rejected claim 6 as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 6 is dependent upon claim 1. For at least the reasons stated above in regard to claim 1, Appellant submits the rejection of claim 2 is in error and therefore respectfully requests reversal of the rejection.

E.   Claim 7

The Examiner rejected claim 7 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta and Rajski under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 7 is dependent upon claim 1. For at least the reasons stated above in regard to claim 1, Appellant submits the rejection of claim 2 is in error and therefore respectfully requests reversal of the rejection.

F.   Claims 8 and 10

The Examiner rejected claims 8 and 10 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Independent claim 8 recites:

"A built-in self-test controller, comprising:

means for executing a logic built-in self-test, including a pattern generator seeded with a first primitive polynomial; and means for storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial; wherein the first polynomial has a first number of bits and the second polynomial has a second number of bits, wherein the second number is different from the first number" (Emphasis added)

In the Final Office Action, the Examiner admits that McNamara and Kim fail to teach the first and second polynomials being a certain number of bits, wherein the second polynomial has a number of bits different from the first. The Examiner also notes that Pouya suggests the polynomials be different polynomials, but does not specifically state they be different in the number of bits. However, the Examiner asserts that Pouya boasts of reduced test cost in column 1, lines 35-40, and further asserts that motivated as suggested, one with ordinary skill in the art would add the variable polynomial capabilities to the McNamara and Kim references in order to decrease test costs. Appellant submits that this suggestion by Pouya is not equivalent to a suggestion of first and second primitive polynomials having different numbers of bits, as recited in the independent claims.

The Examiner further states in the Final Office Action that Udawatta does teach the feature of a first primitive polynomial having a different number of bits than a second primitive polynomial, and cites Udawatta at column 2, lines 17-67 and column 3, lines 59-61. Column 3, lines 59-61 of Udawatta states:

"Also, the invention can support MISRs with different polynomial sizes by the ability to add more logic and flip flops to store larger polynomials." (Emphasis added).

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While the above citation may teach MISRs that support different polynomial sizes, this citation is silent as to whether these different polynomial sizes are present in the same embodiment or in different embodiments. Appellant notes that the citation appears to suggest enlarging the MISRs by adding more logic and flip-flops for the purpose of storing larger polynomials, but submits that the citation does not suggest an embodiment having two or more MISRs of different sizes. Furthermore, Appellant notes that while the citation above states that MISRs can support different polynomial sizes (and thus may support variation in the size of a second primitive polynomial), Udawatta is silent about the size of the LFSR, any relation between the size of the LSFR and the plurality of MISRs, or the size of a first primitive polynomial stored within an LSFR. Accordingly, Appellant submits that Udawatta does not teach or suggest first and second primitive polynomials of different sizes as recited in the independent claims, and further submits that the cited references, taken singly or in combination do not teach or suggest all of the elements of the independent claims.

Appellant further notes that, in supporting the rejection, the Examiner cites column 3, lines 16-19 of Udawatta, which states:

"Also, one can address the issue of aliasing by <u>increasing the length of the MISR,</u> which has the effect of minimizing the aliasing effect." (Emphasis added).

However, column 1, line 65 to column 2, line 6 of Kim states:

"Since the number of flip-flops in the conventional BIST circuit, implemented using the LFSR and the MISR circuits of FIGS. 1 and 2, is dependant upon the number of inputs and outputs of the circuit to be tested, a circuit to be tested having a large number of inputs and outputs will require a corresponding large number of flip-flops on the LFSR and MISR test circuits. <u>Consequently, the circuit real estate or overhead required for such a BIST circuit increases dramatically.</u>" (Emphasis added).

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MPEP 2141.02 states that the prior art must be considered in its entirety, including disclosures that teach away from the claims. MPEP 2145 (X)(D)(2) states that references cannot be combined where the references teach away from their combination. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. In light of the above citations from Udawatta and Kim, as well as column 4, lines 32-37 of Kim, which states:

> "As described above, according to the present invention, the BIST circuit is implemented using the LFSR and the MISR which share a memory built in a circuit to be tested, and thus the area of the BIST circuit can be greatly reduced regardless of the number of inputs and outputs of the circuit to be tested." (Emphasis added),

Appellant submits that Udawatta and Kim teach away from their combination with each other and further submits that a combination of references including both Udawatta and Kim renders Kim unsatisfactory for its intended purpose (reducing the area required by the BIST circuit). Accordingly, Appellant submits that there is no suggestion or motivation to combine these references.

For at least these reasons, Appellant submits that the rejection of claim 8, as well as that of claim 10 (which depends from claim 8) is in error, and therefore respectfully requests reversal of the rejection.

G.   Claim 9

The Examiner rejected claim 9 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta and Bardell under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

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Appellant notes that claim 9 is dependent upon claim 8. For at least the reasons stated above in regard to claim 8, Appellant submits the rejection of claim 9 is in error and therefore respectfully requests reversal of the rejection.

H.   Claim 11

The Examiner rejected claim 11 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta and Rajski under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 11 is dependent upon claim 8. For at least the reasons stated above in regard to claim 8, Appellant submits the rejection of claim 11 is in error and therefore respectfully requests reversal of the rejection.

I.   Claims 12, 14, 16, 17, and 18

The Examiner rejected claims 12, 14, 16, 17, and 18 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta and Motika under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Independent claim 12 recites, in pertinent part:

"a built-in self-test controller, including ... a pattern generator seeded with a first primitive polynomial; and a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial; wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number" (Emphasis added).

In the Final Office Action, the Examiner admits that McNamara and Kim fail to teach the first and second polynomials being a certain number of bits, wherein the second

polynomial has a number of bits different from the first. The Examiner also notes that Pouya suggests the polynomials be different polynomials, but does not specifically state they be different in the number of bits. However, the Examiner asserts that Pouya boasts of reduced test cost in column 1, lines 35-40, and further asserts that motivated as suggested, one with ordinary skill in the art would add the variable polynomial capabilities to the McNamara and Kim references in order to decrease test costs. Appellant submits that this suggestion by Pouya is not equivalent to a suggestion of first and second primitive polynomials having different numbers of bits, as recited in the independent claims.

The Examiner further states in the Final Office Action that Udawatta does teach the feature of a first primitive polynomial having a different number of bits than a second primitive polynomial, and cites Udawatta at column 2, lines 17-67 and column 3, lines 59-61. Column 3, lines 59-61 of Udawatta states:

"Also, the invention can support MISRs <u>with different polynomial sizes by the ability to add more logic and flip flops</u> to store larger polynomials." (Emphasis added).

While the above citation may teach MISRs that support different polynomial sizes, this citation is silent as to whether these different polynomial sizes are present in the same embodiment or in different embodiments. Appellant notes that the citation appears to suggest enlarging the MISRs by adding more logic and flip-flops for the purpose of storing larger polynomials, but submits that the citation does not suggest an embodiment having two or more MISRs of different sizes. Furthermore, Appellant notes that while the citation above states that MISRs can support different polynomial sizes (and thus may support variation in the size of a second primitive polynomial), Udawatta is silent about the size of the LFSR, any relation between the size of the LSFR and the plurality of MISRs, or the size of a first primitive polynomial stored within an LSFR. Accordingly, Appellant submits that Udawatta does not teach or suggest first and second primitive

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polynomials of different sizes as recited in the independent claims, and further submits that the cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims.

Appellant further notes that, in supporting the rejection, the Examiner cites column 3, lines 16-19 of Udawatta, which states:

"Also, one can address the issue of aliasing by increasing the length of the MISR, which has the effect of minimizing the aliasing effect." (Emphasis added).

However, column 1, line 65 to column 2, line 6 of Kim states:

"Since the number of flip-flops in the conventional BIST circuit, implemented using the LFSR and the MISR circuits of FIGS. 1 and 2, is dependant upon the number of inputs and outputs of the circuit to be tested, a circuit to be tested having a large number of inputs and outputs will require a corresponding large number of flip-flops on the LFSR and MISR test circuits. Consequently, the circuit real estate or overhead required for such a BIST circuit increases dramatically." (Emphasis added).

MPEP 2141.02 states that the prior art must be considered in its entirety, including disclosures that teach away from the claims. MPEP 2145 (X)(D)(2) states that references cannot be combined where the references teach away from their combination. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. In light of the above citations from Udawatta and Kim, as well as column 4, lines 32-37 of Kim, which states:

"As described above, according to the present invention, the BIST circuit is implemented using the LFSR and the MISR which share a memory built in a circuit to be tested, and thus the area of the BIST circuit can be greatly reduced

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regardless of the number of inputs and outputs of the circuit to be tested." (Emphasis added),

Appellant submits that Udawatta and Kim teach away from their combination with each other and further submits that a combination of references including both Udawatta and Kim renders Kim unsatisfactory for its intended purpose (reducing the area required by the BIST circuit). Accordingly, Appellant submits that there is no suggestion or motivation to combine these references.

For at least these reasons, Appellant submits that the rejection of claim 12, as well as claims 14, 16, 17, and 18 (which depend from claim 12) is in error, and therefore respectfully requests reversal of the rejection.

J.   Claim 13

The Examiner rejected claim 13 as being unpatentable over over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika and Bardell under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 13 is dependent upon claim 12. For at least the reasons stated above in regard to claim 12, Appellant submits the rejection of claim 13 is in error and therefore respectfully requests reversal of the rejection.

K.   Claim 15

The Examiner rejected claim 15 as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant submits that the cited references, taken singly or in combination, do not teach or suggest all of the elements of claim 15, which in pertinent part recites:

"a step state entered into from the scan state and from <u>which the scan state is
entered</u> **unless** <u>the content of the pattern generator equals a predetermined</u> **vector
count**" (Emphasis added).

In the Final Office Action, the Examiner asserts that Wong teaches the states of
scan, step, and complete in column 6, lines 26-50. Column 6, lines 26-50 of Wong states:

"Referring to FIG. 4, a flow diagram for a preferred process 400 of operating the
system 100 in accordance with the present invention is shown. After the start 402
of the process 400, the scan path initializes 404 the state elements of the scan
registers by flushing the scan path. During initialization, the state elements in the
LRSCs 108.sub.1, 108.sub.2 and LNSCs 110.sub.1, 110.sub.2 are flushed to a
zero state. This ensures that the last scan register 106.sub.6 in the functional path
is in a 1-hot or 1-cold condition. Upon completion of initialization, the process
400 then disables update of all the LRSCs 406 by holding the clock enable off for
state elements in the LRSCs 108.sub.1, 108.sub.2.

The process then performs 408 a certain number of system clocks to establish
partially decoded values in the functional path based on an all zero encoded state.
The PRPG 102 feeds 410 random data to the LRSCs 108.sub.1, 108.sub.2, but not
to the LNSCs 110.sub.1, 110.sub.2. The process 400 then runs 412 the LBIST
sequences until complete. The MISR 114 receives bit values which indicate test
responses and produces 414 a unique signature. As shown in step 417, if the test
is not completed, the process returns to step 410 to repeat the process until it is
completed. The signature may be examined to determine the condition of the
system 100, which ends 416 process 400."

The Examiner further states in the Final Office Action that Bogholtz teaches
ending the BIST under the condition of comparing the pattern generator to a pre-set

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count, citing Fig. 10, 32, and column 8, lines 27-40. Column 8, lines 27-40 of Bogholtz states:

"Additionally, FIG. 10 illustrates circuitry that can be employed to allow for generation of the all zeros data pattern. A comparator 32 is implemented to receive and compare the outputs of the start register 18 and counter/LFSR 20. When the comparator 32 determines that the generated data pattern developed by the counter/LFSR 20 is the same as the seed data pattern, then zero output circuitry 34 forces the generated data pattern in the counter/LFSR 20 to all zeros. Further, when an all zeros data pattern is generated, the control circuitry can be programmed to send the next load control signal to the start register 18 one cycle later. Thus, the zero data pattern can be generated without skipping any data patterns in the predetermined sequence."

Appellant can find no teaching or suggestion of the step state as recited in claim 15 anywhere in Wong or Bogholtz, including in the above citations. In particular, Appellant can find no teaching or suggestion of a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count. Appellant further submits that none of the cited references, taken singly or in combination teach or suggest this limitation and that none of the cited references provides a teaching, suggestion, or motivation for adding this limitation and thus obtaining the combination of features recited in claim 15.

In addition to the reasons above, Appellant notes that claim 15 depends from claim 12 and is thus also believed allowable for the reasons stated above in regard to claim 12.

For at least these reasons, Appellant submits that the rejection of claim 15 is in error, and respectfully requests reversal of the rejection.

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L. Claim 19

The Examiner rejected claim 19 as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika and Kim2 under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks

Appellant notes that claim 19 is dependent upon claim 12. For at least the reasons stated above in regard to claim 12, Appellant submits the rejection of claim 19 is in error and therefore respectfully requests reversal of the rejection.

M. Claim 20

The Examiner rejected claim 20 as being unpatentable over McNamara in view of Kim, Pouya, and Udawatt and in further view of Motika and Au under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 20 is dependent upon claim 12. For at least the reasons stated above in regard to claim 12, Appellant submits the rejection of claim 20 is in error and therefore respectfully requests reversal of the rejection.

N. Claim 21

The Examiner rejected claim 21 as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika and Rajski under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 21 is dependent upon claim 12. For at least the reasons stated above in regard to claim 12, Appellant submits the rejection of claim 21 is in error and therefore respectfully requests reversal of the rejection.

O. Claims 22, 24, and 25

The Examiner rejected claims 22, 24, and 25 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Independent claim 22 recites

"A method for performing a logic built-in self-test, the method comprising: seeding a pattern generator in a logic built-in self-test engine with a first primitive polynomial; and executing a logic built-in self-test using the contents of the pattern generator; and storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial; wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number" (Emphasis added)

In the Final Office Action, the Examiner admits that McNamara and Kim fail to teach the first and second polynomials being a certain number of bits, wherein the second polynomial has a number of bits different from the first. The Examiner also notes that Pouya suggests the polynomials be different polynomials, but does not specifically state they be different in the number of bits. However, the Examiner asserts that Pouya boasts of reduced test cost in column 1, lines 35-40, and further asserts that motivated as suggested, one with ordinary skill in the art would add the variable polynomial capabilities to the McNamara and Kim references in order to decrease test costs. Appellant submits that this suggestion by Pouya is not equivalent to a suggestion of first and second primitive polynomials having different numbers of bits, as recited in the independent claims.

The Examiner further states in the Final Office Action that Udawatta does teach the feature of a first primitive polynomial having a different number of bits than a second primitive polynomial, and cites Udawatta at column 2, lines 17-67 and column 3, lines 59-61. Column 3, lines 59-61 of Udawatta states:

"Also, the invention can support MISRs <u>with different polynomial sizes by the ability to add more logic and flip flops</u> to store larger polynomials." (Emphasis added).

While the above citation may teach MISRs that support different polynomial sizes, this citation is silent as to whether these different polynomial sizes are present in the same embodiment or in different embodiments. Appellant notes that the citation appears to suggest enlarging the MISRs by adding more logic and flip-flops for the purpose of storing larger polynomials, but submits that the citation does not suggest an embodiment having two or more MISRs of different sizes. Furthermore, Appellant notes that while the citation above states that MISRs can support different polynomial sizes (and thus may support variation in the size of a second primitive polynomial), Udawatta is silent about the size of the LFSR, any relation between the size of the LSFR and the plurality of MISRs, or the size of a first primitive polynomial stored within an LSFR. Accordingly, Appellant submits that Udawatta does not teach or suggest first and second primitive polynomials of different sizes as recited in the independent claims, and further submits that the cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims.

Appellant further notes that, in supporting the rejection, the Examiner cites column 3, lines 16-19 of Udawatta, which states:

"Also, one can address the issue of aliasing by <u>increasing the length of the MISR,</u> which has the effect of minimizing the aliasing effect." (Emphasis added).

However, column 1, line 65 to column 2, line 6 of Kim states:

"Since the number of flip-flops in the conventional BIST circuit, implemented using the LFSR and the MISR circuits of FIGS. 1 and 2, is dependant upon the number of inputs and outputs of the circuit to be tested, a circuit to be tested

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having a large number of inputs and outputs will require a corresponding large number of flip-flops on the LFSR and MISR test circuits. <u>Consequently, the circuit real estate or overhead required for such a BIST circuit increases dramatically.</u>" (Emphasis added).

MPEP 2141.02 states that the prior art must be considered <u>in its entirety</u>, including disclosures that teach away from the claims. MPEP 2145 (X)(D)(2) states that <u>references cannot be combined where the references teach away from their combination</u>. MPEP 2143.01 states that the proposed modification <u>cannot render the prior art unsatisfactory for its intended purpose</u>. In light of the above citations from Udawatta and Kim, as well as column 4, lines 32-37 of Kim, which states:

"As described above, according to the present invention, the BIST circuit is implemented using the LFSR and the MISR which share a memory built in a circuit to be tested, <u>and thus the area of the BIST circuit can be greatly reduced</u> regardless of the number of inputs and outputs of the circuit to be tested." (Emphasis added),

Appellant submits that Udawatta and Kim teach away from their combination with each other and further submits that a combination of references including both Udawatta and Kim renders Kim unsatisfactory for its intended purpose (reducing the area required by the BIST circuit). Accordingly, Appellant submits that there is no suggestion or motivation to combine these references.

For at least these reasons, Appellant submits that the rejection of claim 22, as well as claims 24 and 25 (which depend from claim 22) is in error, and therefore respectfully requests reversal of the rejection.

P.   Claim 23

The Examiner rejected claim 23 as being unpatentable over McNamara in view of Pouya and Kim and in further view of Udawatta and Bardell under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 23 is dependent upon claim 22. For at least the reasons stated above in regard to claim 22, Appellant submits the rejection of claim 23 is in error and therefore respectfully requests reversal of the rejection.

Q.   Claim 26

The Examiner rejected claim 26 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Udawatta, Wong, and Bogholtz under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Claim 26 recites, in pertinent part:

"scanning a scan chain upon the initialization of the components and the signals; stepping to a new scan chain; and repeating the previous scanning and stepping until the content of the pattern generator equals a predetermined vector count" (Emphasis added).

In the Final Office Action, the Examiner asserts that Wong teaches the states of scan, step, and complete in column 6, lines 26-50. Column 6, lines 26-50 of Wong states:

"Referring to FIG. 4, a flow diagram for a preferred process 400 of operating the system 100 in accordance with the present invention is shown. After the start 402 of the process 400, the scan path initializes 404 the state elements of the scan registers by flushing the scan path. During initialization, the state elements in the LRSCs 108.sub.1, 108.sub.2 and LNSCs 110.sub.1, 110.sub.2 are flushed to a zero state. This ensures that the last scan register 106.sub.6 in the functional path is in a 1-hot or 1-cold condition. Upon completion of initialization, the process

400 then disables update of all the LRSCs 406 by holding the clock enable off for state elements in the LRSCs 108.sub.1, 108.sub.2.

The process then performs 408 a certain number of system clocks to establish partially decoded values in the functional path based on an all zero encoded state. The PRPG 102 feeds 410 random data to the LRSCs 108.sub.1, 108.sub.2, but not to the LNSCs 110.sub.1, 110.sub.2. The process 400 then runs 412 the LBIST sequences until complete. The MISR 114 receives bit values which indicate test responses and produces 414 a unique signature. As shown in step 417, if the test is not completed, the process returns to step 410 to repeat the process until it is completed. The signature may be examined to determine the condition of the system 100, which ends 416 process 400."

The Examiner further states in the Final Office Action that Bogholtz teaches ending the BIST under the condition of comparing the pattern generator to a pre-set count, citing Fig. 10, 32, and column 8, lines 27-40. Column 8, lines 27-40 of Bogholtz states:

"Additionally, FIG. 10 illustrates circuitry that can be employed to allow for generation of the all zeros data pattern. A comparator 32 is implemented to receive and compare the outputs of the start register 18 and counter/LFSR 20. When the comparator 32 determines that the generated data pattern developed by the counter/LFSR 20 is the same as the seed data pattern, then zero output circuitry 34 forces the generated data pattern in the counter/LFSR 20 to all zeros. Further, when an all zeros data pattern is generated, the control circuitry can be programmed to send the next load control signal to the start register 18 one cycle later. Thus, the zero data pattern can be generated without skipping any data patterns in the predetermined sequence."

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Appellant can find no teaching or suggestion of repeating the previous scanning and stepping until the content of the pattern generator equals a <u>predetermined vector count</u> as recited in claim 26 anywhere in Wong or Bogholtz, including in the above citations. Appellant further submits that none of the cited references, taken singly or in combination teach or suggest this limitation and that none of the cited references provides a teaching, suggestion, or motivation for adding this limitation and thus obtaining the combination of features recited in claim 26.

In addition to the reasons above, Appellant notes that claim 26 depends from claim 22 and is thus also believed allowable for the reasons stated above in regard to claim 22.

For at least these reasons, Appellant submits that the rejection of claim 26 is in error, and respectfully requests reversal of the rejection.

R.   Claim 27

The Examiner rejected claim 27 as being unpatentable over McNamara in view of Kim, Pouya, and Udawatta and in further view of Motika under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 27 is dependent upon claim 22. For at least the reasons stated above in regard to claim 22, Appellant submits the rejection of claim 27 is in error and therefore respectfully requests reversal of the rejection.

S.   Claim 28

The Examiner rejected claim 28 as being unpatentable over McNamara in view of Kim and Pouya and in further view of Rajski under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 28 is dependent upon claim 22. For at least the reasons stated above in regard to claim 22, Appellant submits the rejection of claim 28 is in error and therefore respectfully requests reversal of the rejection.

T. **Claims 29, 31, 32, and 33**

The Examiner rejected claims 29, 31, 32, and 33 as being unpatentable over Rajski, Kim, and Pouya and in further view of Udawatta under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Independent claim 29 recites, in pertinent part:

"seeding a pattern generator in a logic built-in self-test engine with a first primitive polynomial; executing a logic built-in self-test using the contents of the pattern generator; and storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial; and reading the stored results; wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number" (Emphasis added).

In the Final Office Action, the Examiner admits that McNamara and Kim fail to teach the first and second polynomials being a certain number of bits, wherein the second polynomial has a number of bits different from the first. The Examiner also notes that Pouya suggests the polynomials be different polynomials, but does not specifically state they be different in the number of bits. However, the Examiner asserts that Pouya boasts of reduced test cost in column 1, lines 35-40, and further asserts that motivated as suggested, one with ordinary skill in the art would add the variable polynomial capabilities to the McNamara and Kim references in order to decrease test costs. Appellant submits that this suggestion by Pouya is not equivalent to a suggestion of first and second primitive polynomials having different numbers of bits, as recited in the independent claims.

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The Examiner further states in the Final Office Action that Udawatta does teach the feature of a first primitive polynomial having a different number of bits than a second primitive polynomial, and cites Udawatta at column 2, lines 17-67 and column 3, lines 59-61. Column 3, lines 59-61 of Udawatta states:

"Also, the invention can support MISRs <u>with different polynomial sizes by the ability to add more logic and flip flops</u> to store larger polynomials." (Emphasis added).

While the above citation may teach MISRs that support different polynomial sizes, this citation is silent as to whether these different polynomial sizes are present in the same embodiment or in different embodiments. Appellant notes that the citation appears to suggest enlarging the MISRs by adding more logic and flip-flops for the purpose of storing larger polynomials, but submits that the citation does not suggest an embodiment having two or more MISRs of different sizes. Furthermore, Appellant notes that while the citation above states that MISRs can support different polynomial sizes (and thus may support variation in the size of a second primitive polynomial), Udawatta is silent about the size of the LFSR, any relation between the size of the LSFR and the plurality of MISRs, or the size of a first primitive polynomial stored within an LSFR. Accordingly, Appellant submits that Udawatta does not teach or suggest first and second primitive polynomials of different sizes as recited in the independent claims, and further submits that the cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims.

Appellant further notes that, in supporting the rejection, the Examiner cites column 3, lines 16-19 of Udawatta, which states:

"Also, one can address the issue of aliasing by <u>increasing the length of the MISR,</u> which has the effect of minimizing the aliasing effect." (Emphasis added).

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However, column 1, line 65 to column 2, line 6 of Kim states:

"Since the number of flip-flops in the conventional BIST circuit, implemented using the LFSR and the MISR circuits of FIGS. 1 and 2, is dependant upon the number of inputs and outputs of the circuit to be tested, a circuit to be tested having a large number of inputs and outputs will require a corresponding large number of flip-flops on the LFSR and MISR test circuits. Consequently, the circuit real estate or overhead required for such a BIST circuit increases dramatically." (Emphasis added).

MPEP 2141.02 states that the prior art must be considered in its entirety, including disclosures that teach away from the claims. MPEP 2145 (X)(D)(2) states that references cannot be combined where the references teach away from their combination. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. In light of the above citations from Udawatta and Kim, as well as column 4, lines 32-37 of Kim, which states:

"As described above, according to the present invention, the BIST circuit is implemented using the LFSR and the MISR which share a memory built in a circuit to be tested, and thus the area of the BIST circuit can be greatly reduced regardless of the number of inputs and outputs of the circuit to be tested." (Emphasis added),

Appellant submits that Udawatta and Kim teach away from their combination with each other and further submits that a combination of references including both Udawatta and Kim renders Kim unsatisfactory for its intended purpose (reducing the area required by the BIST circuit). Accordingly, Appellant submits that there is no suggestion or motivation to combine these references.

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For at least these reasons, Appellant submits that the rejection of claim 29, as well as claims 31, 32, and 33 (which depend from claim 29) is in error, and therefore respectfully requests reversal of the rejection.

U.   Claim 30

The Examiner rejected claim 30 as being unpatentable over Au in view of Rajski and Kim and in further view of Bardell under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.
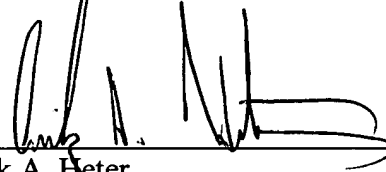
Appellant notes that claim 30 is dependent upon claim 29. For at least the reasons stated above in regard to claim 29, Appellant submits the rejection of claim 30 is in error and therefore respectfully requests reversal of the rejection.

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VII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-33 was erroneous, and reversal of his decision is respectfully requested.

Respectfully submitted,

Erik A. Heter
Reg. No. 50,652
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 4/28/05

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IX.   APPENDIX

The claims on appeal are as follows.

1.   A built-in self-test controller, comprising:

a logic built-in self-test engine capable of executing a logic built-in self-test, including:

    a logic built-in self-test state machine; and

    a pattern generator seeded with a first primitive polynomial; and

    a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial;

wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

2.   The built-in self-test controller of claim 1, wherein the first primitive polynomial is $x^{31} + x^3 + 1$.

3.   The built-in self-test controller of claim 1, wherein the second primitive polynomial is $x^{32} + x^{28} + x + 1$.

4.   The built-in self-test controller of claim 1, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into when the content of the pattern generator equals the predetermined vector count.

5.   The built-in self-test controller of claim 1, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

6.   The built-in self-test controller of claim 1, wherein the multiple input signature register includes at least one of:

a bit indicating whether the logic built-in self-test is done;

a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

7.   The built-in self-test controller of claim 1, wherein the seed for the pattern generator is externally configurable.

8.   A built-in self-test controller, comprising:

means for executing a logic built-in self-test, including a pattern generator seeded with a first primitive polynomial; and

means for storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial;

wherein the first polynomial has a first number of bits and the second polynomial has a second number of bits, wherein the second number is different from the first number.

9.   The built-in self-test controller of claim 8, wherein the first primitive polynomial is $x^{31} + x^3 + 1$.

10.   The built-in self-test controller of claim 8, wherein the second primitive polynomial is $x^{32} + x^{28} + x + 1$.

11.   The built-in self-test controller of claim 8, wherein the seed for the pattern generator is externally configurable.

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12.   A integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

a built-in self-test controller, including:

      a logic built-in self-test engine capable of executing a logic built-in self-test and storing the results thereof, including: a logic built-in self-test state machine; and a pattern generator seeded with a first primitive polynomial; and

      a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial;

      wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

13.   The integrated circuit device of claim 12, wherein the first primitive polynomial is $x^{31} + x^3 + 1$.

14.   The integrated circuit device of claim 12, wherein the second primitive polynomial is $x^{32} + x^{28} + x + 1$.

15.   The integrated circuit device of claim 12, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

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a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into when the content of the pattern generator equals the predetermined vector count.

16.   The integrated circuit device of claim 12, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

17.   The integrated circuit device of claim 12, wherein the multiple input signature register includes at least one of:

a bit indicating whether the logic built-in self-test is done; a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

18.   The integrated circuit device of claim 12, further comprising: a memory built-in self-test engine; and

a memory built-in self-test signature register capable of storing the results of the memory built-in self-test.

19.   The integrated circuit device of claim 12, wherein the memory components include a static random access memory device.

20.   The integrated circuit device of claim 12, wherein testing interface comprises a Joint Test Action Group tap controller.

21.   The integrated circuit device of claim 12, wherein the seed for the pattern generator is externally configurable.

22.   A method for performing a logic built-in self-test, the method comprising:

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seeding a pattern generator in a logic built-in self-test engine with a first primitive polynomial; and

executing a logic built-in self-test using the contents of the pattern generator; and storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial;

wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

23. The method of claim 22, wherein seeding the pattern generator with the first primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^3 + 1$.

24. The method of claim 23, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial $x^{32} + x^{28} + x + 1$.

25. The method of claim 22, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial $x^{32} + x^{28} + x + 1$.

26. The method of claim 22, wherein executing the logic built-in self-test includes:
initiating a plurality of components and signals in a logic built-in self-test domain of a built-in self-test controller upon receipt of a logic built-in self-test run signal;
scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of the pattern generator equals a predetermined vector count.

27. The method of claim 26, further comprising at least one of:

setting a bit in a multiple input signature register indicating whether the logic built-in self-test is done;

setting a bit in the multiple input signature register indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

28. The method of claim 22, further comprising externally configuring the seed.

29. A method for testing an integrated circuit device, the method comprising:

interfacing the integrated circuit device with a tester;

performing a logic built-in self-test, including:

seeding a pattern generator in a logic built-in self-test engine with a first primitive polynomial;

executing a logic built-in self-test using the contents of the pattern generator; and

storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial; and reading the stored results;

wherein the first primitive polynomial has a first number of bits and the second primitive polynomial has a second number of bits, wherein the second number is different from the first number.

30. The method of claim 29, wherein seeding the pattern generator with the first primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^3 + 1$.

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31. The method of claim 29, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial $x^{32} + x^{28} + x + 1$.

32. The method of claim 29, further comprising externally configuring the seed.

33. The method of claim 29, further comprising performing a memory built-in self-test.

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X. EVIDENCE APPENDIX

No evidence submitted under 37 C.F.R. §§ 1.130, 1.131, or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

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XI.   RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

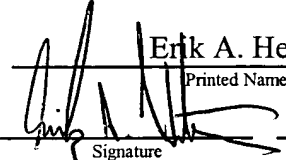Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 09/976,708	Examiner: Trimmings, J.
Filed: October 12, 2001	Group/Art Unit: 2133
Inventor(s):	Atty. Dkt. No: 5681-55500
Michael C. Dorsey	

Title: ASIC LOGIC BIST
EMPLOYING REGISTERS
SEEDED WITH
DIFFERING PRIMITIVE
POLYNOMIALS

§ § § § § § § § § § § § § §

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Erik A. Heter
Printed Name

_____   4/28/05
Signature   Date

FEE AUTHORIZATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The Commissioner is hereby authorized to charge the following fee to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 50-1505/5681-55500/BNK:

Fee:	Appeal Brief
Amount:	$500.00
Attorney Docket No.:	5681-55500

The Commissioner is also authorized to charge any extension fee or other fees, which may be necessary to the same account number.

Respectfully submitted,

Erik A. Heter
Reg. No. 50,652
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800
Date: April 28, 2005